

WHAT IS CLAIMED IS:

1 1. A processing core for executing instructions, comprising:
2 a first source register including a plurality of source fields;
3 a second source register including a plurality of result field select values
4 and a plurality of operation fields;
5 a multiplexer coupled to at least one of the source fields;
6 a destination register including a plurality of result fields; and
7 an operand processor coupled to at least one of the result fields, wherein
8 the operand processor and multiplexer operate upon at least one of the plurality of source
9 fields.

1 2. The processing core of claim 1, wherein:
2 the multiplexer includes a mux input, a select input and a mux output; and
3 the operand processor includes a processor input, a processor output and a
4 condition input.

1 3. The processing core for executing instructions of claim 2, wherein
2 the mux input is coupled to at least one of the source fields.

1 4. The processing core for executing instructions of claim 2, wherein
2 the select input is coupled to at least one of the result field select values.

1 5. The processing core for executing instructions of claim 2, wherein
2 the processor input is coupled to the mux output.

1 6. The processing core for executing instructions of claim 2, wherein
2 the condition input is coupled to at least one of the operation fields.

1 7. The processing core for executing instructions of claim 2, wherein
2 the processor output is coupled to at least one of the result fields.

1 8. The processing core for executing instructions of claim 1, wherein
2 the operand processor performs an operation selected from a group consisting of:
3 setting each bit from the source field low,
4 extension of a highest order bit of the source field to remaining bits,
5 bitwise inversion of the source field,

4 setting each bit from the source field low,
5 extending a highest order bit of the source field to remaining bits,
6 bitwise inverting the source field,
7 setting each bit of the source field high,
8 inverting the highest order bit of the source field and extending the highest
9 order bit to remaining bits,
10 bitwise reverting the source field,
11 extending the lowest order bit of the source field to remaining bits,
12 bitwise inverting and reverting of the source field, and
13 inverting of the lowest order bit of the source field and extending the
14 inverted highest order bit to remaining bits.

1 13. The method for performing the operation in the data processing
2 machine as recited in claim 10, wherein the source field is eight bits wide.

1 14. A method for performing an operation in a data processing
2 machine, the method comprising steps of:
3 loading a first source field from a source register;
4 loading a second source field from the source register;
5 manipulating the first source field to produce a first result;
6 manipulating the second source field to produce a second result;
7 storing the first result in a second result field of a destination field; and
8 storing the second result in a first result field of the destination field,
9 wherein at least three of the preceding steps are associated with a single issue.

1 15. The method for performing the operation in the data processing
2 machine of claim 14, wherein the result field is eight bits wide.

1 16. The method for performing the operation in the data processing
2 machine of claim 14, wherein the first result is different from the first source field.

1 17. The method for performing the operation in the data processing
2 machine of claim 14, wherein the second result is different from the second source field.

1 18. The method for performing the operation in the data processing
2 machine of claim 14, wherein the manipulation step includes a step selected from a group
3 consisting of:

4 setting each bit from the source field low,
5 extending a highest order bit of the source field to remaining bits,
6 bitwise inverting the source field,
7 setting each bit of the source field high,
8 inverting the highest order bit of the source field and extending the highest
9 order bit to remaining bits,
10 bitwise reverting the source field,
11 extending the lowest order bit of the source field to remaining bits,
12 bitwise inverting and reverting of the source field, and
13 inverting of the lowest order bit of the source field and extending the
14 inverted highest order bit to remaining bits.

1 19. The method for performing the operation in the data processing
2 machine of claim 14, wherein the loading, storing and manipulating steps are part of a
3 same instruction issue.